Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) A latch circuit, comprising:

a bistable pair of transistors connected between a reset switch and a first supply voltage, and having a first port for receiving a first current signal and producing a first output voltage, and a second port for receiving a second current signal and producing a second output voltage; and

a vertical latch having a first transistor and a second transistor and connected between said first supply voltage and a second supply voltage, ~~and connected to said first port, said vertical latch having a~~ said first transistor connected to said first port so that, when said first transistor is turned on, a current flows from said second supply voltage through said first transistor to said first ~~port;~~ port, said first transistor is a first type, said second transistor is a second type, and said first type is different from said second type;

wherein ~~said reset switch is configured to couple said first port directly to said second port and~~ said bistable pair of transistors ~~are~~ is connected directly to said first supply voltage.

2. (Currently Amended) The latch circuit of claim 1, wherein said first transistor is a MOSFET.

3. (Original) The latch circuit of claim 1, wherein said reset switch is a microelectromechanical reset switch.

4. (Previously Presented) The latch circuit of claim 1, wherein said vertical latch is for decreasing the time necessary for said first port to reach a steady state voltage in response to said first current signal received.

5. (Original) The latch circuit of claim 1, further comprising a vertical latch reset switch connected to said vertical latch.

6. (Original) The latch circuit of claim 1, further comprising a second vertical latch connected between said first supply voltage and said second supply voltage, and connected to said second port.

7-20. (Canceled)

21. (New) A latch circuit, comprising:

a first transistor coupled between a first port and a supply voltage;

a second transistor coupled between a second port and said supply voltage; and

a microelectromechanical reset switch coupled between said first port and said second port;

wherein said first transistor and said second transistor are configured in a bistable pair, said first port is configured to receive a first current signal and to produce a first output

voltage, and said second port is configured to receive a second current signal and to produce a second output voltage.